GE GE □□□ Series Service Manual

DS200TCDAG1BDB

1. Description

DS200TCDAG1BDB Technical Specifications

2. Specifications

Specification	Value
OEM	**General Electric**
Series	**Mark V Speedtronic**
Part	**Number DS200TCDAG1BDB**
Functional	**Abbreviation TCDA**
Assembly	**Type Normal Assembly**
Revision	**Quantity 3 Revisions**
Backwards-Compatibility	**1st two revisions**
About	**the DS200TCDAG1BDB**
GE's	**DS200TCDAG1BDB printed circuit board is a Digital I/O board used within the company's Speedtronic Mark V system. The Mark V was a third-generation triple modular redundant or TMR management system for industrial steam and gas turbine systems.**

3. Product Information

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About the DS200TCDAG1BDB

GE’s DS200TCDAG1BDB printed circuit board is a Digital I/O board used within the company’s Speedtronic Mark V system. The Mark V was a third-generation triple modular redundant or TMR management system for industrial steam and gas turbine systems.

This DS200TCDAG1BDB Digital I/O or Digital Input/Output Board is not the original Digital I/O Board that was first manufactured for General Electric's Mark V Turbine Control System Series; that would be the more-rudimentary DS200TCDAG1 parent printed circuit board missing this specific DS200TCDAG1BDB PCB's three significant product revisions.

Hardware Tips and Specifications

The DS200TCDAG1BDB is used as an interface for contact inputs and relay outputs. Software configuration will help with these. Given this DS200TCDAG1BDB printed circuit board's general intended application of a Digital I/O Board interface, it incorporates many unique and necessary hardware components into its internal assembly. The DS200TCDAG1BDB I/O board works within the Mark V’s <R1> core. Within this core are other boards like:

TCEA

TCQE

TCQA

UCPB

STCA

If you also need to replace these boards, we have them in our inventory. The assembly of this DS200TCDAG1BDB circuit board includes many jumper switches that offer hardware configuration options. These jumpers include the J1 through J8 jumpers; The J4 through J6 jumpers are used for IONET addressing, and should be left at factory settings, while jumper J7 enables stall timer and J8 is for test enable.

The DS200TCDAG1BDB board featured here also contains components like an LED panel, resistor network arrays, pin connectors, integrated circuits, vertical pin plug connectors, capacitors, and relays, most of which have been included in its internal assembly for voltage limiting or reduction purposes. The board is factory-drilled to facilitate mounting options and has been marked along the edge to help with installation alignment. All of these aforementioned hardware components gain at least some level of daily wear and tear protection and insulation from the normal style of PCB coating applied to this DS200TCDAG1BDB circuit board's base board.

SPECIFICATIONS:

Part Number: DS200TCDAG1BDB

Manufacturer: General Electric

Series: Mark V LM

Product Type: Digital I/O Board

Power Requirements: +5 V dc, 6 A

Number of relay channels: 12

Power supply voltage: 28 V dc

Mounting: DIN-rail mounting

Technology: Surface mount

Operating temperature: -30 to +65°C

Size: 15.9 cm high x 17.8 cm

Repair: 3-7 Day

Availability: In Stock

Country of Origin: United States

Manual: GEI-100182B

FUNCTIONAL DESCRIPTION:

DS200TCDAG1BDB is a Digital I/O Board manufactured and designed by General Electric as part of the Mark V LM Series used in GE Speedtronic Control Systems. The Digital IO Board (TCDA) is housed within the digital I/O cores , , and , if applicable. It manages digital contact input signals originating from the DTBA and DTBB terminal boards, as well as contact output signals (relay/solenoid) from the TCRA boards. These signals are relayed via the IONET to the TCQC board in and , or to the CTBA terminal board in when is included.

TCDA CONFIGURATION:

HARDWARE: The TCDA board features eight hardware jumpers with specific functions. J1 and J8 are designated for factory testing, while J2 and J3 handle IONET termination resistors. Jumpers J4, J5, and J6 configure the board's IONET ID, and J7 enables the stall timer. For detailed hardware jumper settings, consult Appendix A and the operator interface's hardware jumper screen.

SOFTWARE: The I/O Configuration Editor on the HMI is used to input constants for contact input inversions, as detailed below.

TCDA CONNECTORS:

JP: Distributes power from the TCPS board in the R1, R2, and R5 cores to the Q11, Q21, and Q51 cores, respectively.

JQ: Connects to the JQR socket on the DTBA board, transmitting contact input signals from the DTBA board to the TCDA board.

JR: Connects to the JRR socket on the DTBB board, conveying contact input signals from the DTBB board to the TCDA board.

JO1: Transmits contact output (relay/solenoid) signals to the TCRA board in location four. Not utilized in Q11, as the relays in location 4 are directly controlled by TCQE in R1.

JO2: Transmits contact output (relay/solenoid) signals to the TCRA board in location five.

JX1: This is a shielded twisted pair cable for IONET signals. The TCDA board in the Q11 core sends signals to the JX2 connection on the TCEA board in location five of the P1 core.

JX2: Used for the same function as JX1. Either JX1 or JX2 can be employed for this purpose.